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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,388	12/10/2003	Ramachandra Divakaruni	FIS920030274	1387

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EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
10/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,388	DIVAKARUNI ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Dictionary citation*.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 12-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "damaging temperature" in claim 12 renders the claim indefinite. The term "damaging temperature" is defined as "a temperature at which damage is probable to occur in any of the plurality of BEOL layers" (Specification, ¶19). The term "probable" is not defined by the specification, therefore the ordinary definition of "establishing a probability" has been applied (see attachment from Webster's Dictionary). Because the specification does not establish a probability of damage at the silicidation temperature, it is not sufficiently clear whether or not damage occurs to the BEOL layers. Thus one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. In so far as definite, claims 12 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiiki et al. '879 in view of Buskirk '175, and further in view of Krishnan et al. '551.

By both the conventional definition in the art and by the Applicant's definition provided in the specification, a back-end-of-line (BEOL) layer can comprise an ILD layer (Applicant's specification, ¶16, "ILD layer may be any BEOL layer...containing a via and/or metal.") or a metal layer (Applicant's specification, ¶18, "conventional BEOL wiring structure could be...a via to underlying wiring layers or a simple wire."), so long as the layer is formed over the front-end-of-line (FEOL) structures found on a silicon substrate. Shiiki et al. discloses a semiconductor device (¶45-51; fig. 1A) comprising a silicide resistor (2) in one of a plurality of BEOL layers (3 & 2). The reference discloses an interlayer dielectric (ILD, 3) and a silicide resistor layer (2) formed over FEOL structures (13).

Shiiki further discloses the silicide resistor to include a silicide section including molybdenum silicide or tungsten silicide (¶51); a polysilicon base positioned below the silicide section (¶51; resistor formed of refractory metal in addition to the polysilicon layer); and wherein the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers.

Shiiki discloses a preferable temperature of 450 °C to form the resistor (¶51). This is read as a silicidation temperature less than a damaging temperature of the plurality of BEOL layers in light of the facts that: a) the structure is built at this temperature and operates as intended, thereby meaning the BEOL layer (3) was sufficiently undamaged during the silicide formation process, and b) the

Applicant's specification gives illustrative examples (species) of silicidation temperatures less than a damaging temperature of the plurality of BEOL layers (genus) that are of 600 °C or less, therefore the temperature species of 450 °C reads on the broad genus of "silicidation temperatures less than a damaging temperature of the plurality of BEOL layers".

Shiiki does not explicitly disclose the silicide section to be positioned in a trough in one of the BEOL layers. Buskirk teaches a semiconductor device comprising a silicide resistor (fig. 1E, 30A; ¶13, damascene resistor made of silicide) positioned in a trough in one of a plurality of back-end-of-line (BEOL) layers (20 is formed over substrate 10, which is disclosed to have front-end-of line (FEOL) structures such as transistors, ¶15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to position the silicide resistor of Shiiki in a trough as taught by Buskirk. One would have been motivated to do this because Buskirk taught that depositing conductive material in a trough and polishing back the material (damascene processing) was more advantageous than patterning techniques involving photoresist (e.g., liftoff or photo-etching) because damascene processing avoids the contact of photoresist to the conductive material (¶12). Krishnan taught that patterning conductive material by a damascene process without the use of photolithography was desirable because photoresist consumes time and resources, and because photoresist contaminates the conductive material from particulates and etchant solutions (col. 1, line 60 – col. 2, line 25).

5. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiiki et al. '879 in view of Buskirk '175, further in view of Krishnan et al. '551 and further in view of Wolf, Vol. II (NPL Reference "U", previously provided).

Shiiki et al. in view of Buskirk, and further in view of Krishnan discloses all of the elements of the claims as discussed above including a resistor comprising a silicide section positioned in one of a plurality of BEOL layers, wherein the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers, but the references does not explicitly teach the use of group VIII metals as the silicide material.

Wolf teaches the use of group VIII silicides, including cobalt, palladium, platinum, and nickel silicide, in BEOL resistors (Wolf defines "multilevel interconnects" to include ILD layers, vias, and metal lines (p. 176), thereby meaning BEOL layers as defined above; and because interconnects inherently have a resistance, they are classified as "resistors"). Wolf also teaches the inherent resistivity associated with each silicide (p. 193, Table 4.3; p. 146): cobalt silicide has a resistivity between 14-20 μ-ohm/cm (p. 193, Table 4.3); palladium silicide has a resistivity between 25-30 μ-ohm/cm (p. 146); platinum silicide has a resistivity between 26-35 μ-ohm/cm (p. 193, Table 4.3); and nickel silicide has a resistivity of 50 ohm/cm (p. 146). Wolf teaches the silicidation temperature of the group VIII metals as 600 °C or less (p. 146), which reads on a silicidation temperature less than a damaging temperature of the plurality of BEOL layers as defined above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the group VIII silicide material of Wolf in the resistor of Shiiki et al. in view of Buskirk, and further in view of Krishnan. One would have been motivated to do this because the group VIII silicide formation temperatures of 600 °C or less would have allowed a simple self-aligned silicide (salicide) process to be performed. In a salicide process at 600 °C or less, the metal atoms covering the polysilicon base to diffuse into the base and react with it to form a silicide, while the metal that is present on the ILD outside the polysilicon region does not react with the ILD at that temperature (Wolf, p. 146). Thus, the process of making the resistor becomes less complex and more cost effective by performing a simple selective-etch removal of the unreacted metal, leaving only the reacted metal (silicide resistor) behind.

Response to Arguments

6. Applicant's arguments with respect to claims 12-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax

phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJF

Steven J. Fulk
Patent Examiner
Art Unit 2891

October 2, 2007

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
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